Application No.	Applicant(s)
10/644.795	MORITA ET AL.
Examiner	Art Unit
Jeff Piziali	2629
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5. Notice of Informal 6. Interview Summary Paper No./Mail Da 7. Examiner's Amend 8. Examiner's Statem 9. Other	y (PTO-413), ate
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DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Please amend the claims as follows:

IN THE CLAIMS:

Cancel claims 7, 8, 10, 11, 13, 14, 16, 17, 19, 20, 22, and 23.

Election/Restrictions

- 2. Applicants' election of Species II (i.e., claims 1, 3, 9, 15, and 21) in the reply filed on 13 March 2007 is acknowledged. Because applicants did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).
- 3. Claims 4-8, 10-14, 16-20, 22, and 23 were withdrawn (in accordance with Applicants' election of Species II) from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species, there being no allowable generic or linking claim at the time of the Office action mailed on 27 November 2006. Election was made **without** traverse in the reply filed on 13 March 2007.

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- 4. Applicants are reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).
- 5. Claims 1, 3-6, 9, 12, 15, 18, and 21 are allowable. The restriction requirement among species, as set forth in the Office action mailed on 27 November 2006, has been reconsidered in view of the allowability of claims to the elected invention pursuant to MPEP § 821.04(a). The restriction requirement is hereby withdrawn as to any claim that requires all the limitations of an allowable claim.

Claims 4-6, 12, and 18, directed to a display driver circuit which drives signal electrodes of a display device based on gray-scale data, comprising a data input control circuit which controls input of the gray-scale data supplied to the first to Nth [or (M+N)th] shift register blocks; wherein the first to Nth [or (M+1)th to (M+N)th] shift register blocks are disposed in a region on a second direction side of the data input control circuit, shift a given data enable signal input to the first [or (M+1)th] shift register block and output the shifted data enable signal to a shift register block adjacent in the second direction, and hold the first to Nth [or (M+1)th to (M+N)th] gray-scale data, for which mask control is performed by the first to Nth data mask circuits, based on the shifted data enable signal, and wherein the first to Nth [or (M+1)th to (M+N)th] data mask circuits are connected in the second direction in order from the first to Nth [or (M+1)th to (M+N)th] data mask circuit and unmask the first to Nth [or (M+1)th] to (M+N)th] data mask

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circuit, are no longer withdrawn from consideration because the claims require all the limitations of an allowable claim (in this case, elected independent claim 1).

However, claims 7, 8, 10, 11, 13, 14, 16, 17, 19, 20, 22, and 23, not directed to part or all of the aforementioned subject matter, remain withdrawn from consideration because they do not all require all the limitations of an allowable claim.

In view of the above noted withdrawal of the restriction requirement, applicants are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

Once a restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Priority

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

7. The drawings were received on 15 September 2007. These drawings are acceptable.

Allowable Subject Matter

8. Claims 1, 3-6, 9, 12, 15, 18, and 21 (renumbered as claims 1-10) are allowed.

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9. The following is an examiner's statement of reasons for allowance:

The present invention comprises a display driver circuit which drives signal electrodes of a display device based on gray-scale data. The prior art, Kurokawa et al (US 6,130,657 A) discloses a display driver circuit [Fig. 1; ICBLK] which drives signal electrodes [Fig. 1; Y] of a display device [Fig. 5; LCD] based on gray-scale data [Fig. 1; DATA], comprising: first to (M+N)th (M and N are positive integers) shift register blocks [Fig. 1; 301]; a data input control circuit [Fig. 1; 307] which controls input of the gray-scale data supplied to the first to (M+N)th shift register blocks; first to (M+N)th data mask circuits [Fig. 1; 305] which generate first to (M+N)th gray-scale data by performing mask control for the gray-scale data supplied to the first to (M+N)th shift register blocks and output the first to (M+N)th gray-scale data; and a signal electrode driver circuit [Fig. 1; ICBLK] which drives the signal electrodes by using drive voltages corresponding to the first to (M+N)th gray-scale data, the first to (M+N)th gray-scale data being held in the first to (M+N)th shift register blocks [Fig. 1; 301_{ICBLK1-3}], wherein the first to Mth shift register blocks are disposed in a region on a first direction side [Fig. 1; left side] of the data input control circuit, shift a given data enable signal input [Fig. 1; CAR1] to the first shift register block [Fig. 1; 301_{ICBLK1}] and output the shifted data enable signal to a shift register block [Fig. 1; 301_{ICBLK2}] adjacent in a second direction [Fig. 1; to the right] opposite to the first direction, and hold the first to Mth gray-scale data based on the shifted data enable signal, wherein the (M+1)th to (M+N)th shift register blocks [Fig. 1; 301_{ICBLK4-6}] are disposed in a region on the second direction side [Fig. 1; right side] of the data input control circuit, shift a data enable signal input to the (M+1)th shift register block [Fig. 1; 301_{ICBLK4}] from the Mth shift register block [Fig. 1; 301_{ICBLK3}] and output the shifted data enable signal to a shift register block

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adjacent [Fig. 1; 301_{ICBLK5}] in the second direction [Fig. 1; to the right], and hold the (M+1)th to (M+N)th gray-scale data based on the shifted data enable signal, wherein the first to Mth data mask circuits [Fig. 1; 305(1-3)] are connected in the second direction in order from the first to Mth data mask circuit and mask the first to Mth gray-scale data in order from the first to Mth data mask circuit, and wherein the (M+1)th to (M+N)th data mask circuits [Fig. 1; 305(4-6)] are connected in the second direction in order from the (M+1)th to (M+N)th data mask circuit and unmask the (M+1)th to (M+N)th gray-scale data in order from the (M+1)th to (M+N)th data mask circuit (see Column 4, Line 15 - Column 5, Line 47).

However, as argued by the applicants (on Page 16 of the 'Revised Amendment Under 37 C.F.R. 1.111' filed 15 September 2006), the prior art does not expressly teach the subject matter of, first to Mth [or (M+N)th] data mask control circuits which generate first to Mth [or (M+N)th] data mask control signals for performing mask control for the first to Mth [or (M+N)th] gray-scale data; wherein an ath $(1 \le a \le M)$; a is an integer) data mask control circuit generates an ath data mask control signal based on a data enable signal output from an ath shift register block and an ath data mask circuit masks an ath gray-scale data based on the ath data mask control signal, in combination with the remaining features and subject matter of the instantly claimed invention.

This distinct structural and operational arrangement has been incorporated into both pending independent claims (i.e. claims 1 and 9 -- renumbered as claims 1 and 6), thereby rendering them allowable.

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Any comments considered necessary by applicants must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Piziali

24 May 2007